WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor storage device, which is electrically writable and erasable, comprising:

a substrate;

a plurality of element isolation portions which project from the substrate and are disposed at a predetermined interval;

floating electrodes arranged between the element isolation portions; and

an insulating layer laminated on the element isolation portions and the floating electrodes,

wherein an interval between the adjacent floating electrodes is formed greater at the side away from the substrate than at the substrate side.

2. The nonvolatile semiconductor storage device according to claim 1, wherein the interval is formed from a plurality of step portions.

3. The nonvolatile semiconductor storage device according to claim 2, wherein the sum of thickness of respective step portions other than a thickness of a step portion at the most substrate side among the step portions, is 1/3 or more with respect to the sum of the thickness of all of the step portions.

4. The nonvolatile semiconductor storage device according to claim 2, wherein the sum of the outer circumferential length, at the insulating layer side,

of the cross-section of the floating electrode is greater than or equal to 90% with respect to the sum of the cross-section, in the thickness direction and in the transverse direction, of the floating electrode.

5. The nonvolatile semiconductor storage device according to claim 1, wherein a concave portion is formed on a surface, at the side away from the substrate, of the element isolation portion, and the insulating layer is formed in the concave portion.

6. The nonvolatile semiconductor storage device according to claim 5, wherein an area of a face, which is perpendicular to the depth direction, of the concave portion is made narrower from the opening portion to the bottom portion.

7. A method for manufacturing a nonvolatile semiconductor storage device, comprising:

an element isolation portion forming step of forming element isolation portions which project from a substrate on the substrate;

a polycrystalline silicon layer forming step of forming a polycrystalline silicon layer on the substrate and the element isolation portions;

a first mask material forming process of forming a first mask material on the polycrystalline silicon layer;

a first etching process of etching the polycrystalline silicon layer up to a depth at least

greater than or equal to 1/3 of a thickness of the polycrystalline silicon layer, in a region of the top surface of the element isolation portion;

a second mask material forming process of forming a second mask material on the polycrystalline silicon layer;

a second etching process of etching the polycrystalline silicon layer up to the element isolation portion, in a region etched by the first etching process; and

an insulating layer forming process of forming an insulating layer on the element isolation portions and the polycrystalline silicon layer.